Extc - III - Rev. 09/12/16

DE

Q.P. Code : 545401

(3 Hours) **[Total Marks : 80**

N.B. : (1) **Question No. 1** is compulsory.
(2) **Attempt any 3** questions from Q.2 to Q.6.
(3) Figures to the **right** in the bracket indicate **full** marks.
(4) Assume suitable data if necessary.

1.	a)	State basic theorems of Boolean algebra.	**5**
	b)	Compare Mealy and Moore machine	**5**
	c)	Define Noise Margin, Propagation delay, Power Dissipation	**5**
	d)	Design a full adder using half adders and logic Gates	**5**
2.	a)	Prove that NAND and NOR Gates are universal Gates	**10**
	b)	Design a 2-bit comparator and implement using logic Gates	**10**
3.	a)	Design a 4 bit Binary to Grey code converter.	**10**
	b)	Implement the given function using single 4:1 Multiplexer and few logic gates: $F(A, B, C, D) = \Sigma m(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13, 15)$	**10**
4.	a)	What is a universal shift register? Explain its various modes of operation	**10**
	b)	Write a VHDL program to design a 3:8 Decoder.	**10**
5.	a)	Minimize the following expression using Quine McClusky Technique $F(A,B,C,D) = \Sigma m(0,1,2,3,5,7,9,11)$	**10**
	b)	Convert JK FF to T FF and JK FF to D FF	**10**
6.	a)	Explain the working of 3-bit asynchronous counter with proper timing diagram.	**10**
	b)	Write a note on CPLDs.	**10**
